

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 64-090524

(43)Date of publication of application : 07.04.1989

(51)Int.Cl.

H01L 21/205

C30B 25/02

C30B 29/40

H01L 21/76

H01L 29/80

(21)Application number : 62-249443

(71)Applicant : NEC CORP

(22)Date of filing : 01.10.1987

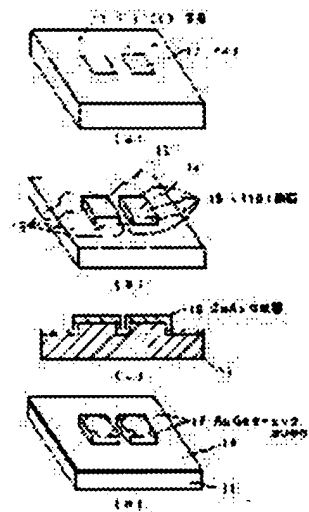
(72)Inventor : IWATA NAOTAKA

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To increase the integration of element on a substrate, by employing a series of processes in which a plateau-shaped structure having both planes (100) and (110) is formed on a IV crystal substrate, and a III-V compound semiconductor layer is then deposited over the substrate body.

CONSTITUTION: First, plateau-shaped structures 14, each of which has both planes (100) and (110), are formed on a IV crystal substrate 11, respectively. Subsequently, a III-V compound semiconductor layer 16 is deposited over the substrate body using an atomic layer epitaxial growth method. Now, a III source gas and a V source gas are alternately supplied to the substrate 11, which provides the atomic layer epitaxial growth of the III-V compound semiconductor. Therefore, the isolation between elements formed on the substrate can be easily performed without the process being complicated. Accordingly, the integration of the element on the substrate can be effectively increased.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]